Tin Dioxide Memristors On Glass And Plastic Substrates

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TIN DIOXIDE MEMRISTORS ON GLASS AND PLASTIC SUBSTRATES

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TIN DIOXIDE MEMRISTORS ON GLASS AND PLASTIC SUBSTRATES

by

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THESIS

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Abstract

NanoMIL has studied and developed SnO$_2$-based memristors, while the W.M Keck Center has been a research leader in printed silver inks. The focus of this thesis is to take the previous generation of memristors on glass and develop a process for creating memristors on flexible Kapton film for the first time. Moreover, collaborative work between the two UTEP laboratories produced memristors with printed silver top electrode contacts, also for the first time. These approaches may enable inexpensive flexible memory.

Maturation of the process was achieved by understanding important process parameters and subtle differences between glass and Kapton substrates. Moreover, electrical characterization of SnO$_2$ memristors on both substrates yielded similar results although yield on the Kapton substrates was lower due to scratches on the Kapton film. Structural and optical characterization was also performed to further understand the active layer in the memristor: The tin dioxide. At last, preliminary results with the printed contacts are presented.
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1. Introduction

1.1. MEMORY EVOLUTION

In the electronics industry, one of the major needs and a must for almost all electronics is the use of memory. Memory has the major functions of storing data such as documents, videos or music. It also stores executing code like firmware and BIOS. The range of needs, as well as costs, has caused a proliferation of different memory types available depending on what is required.

The personal computer and server markets that drive consumption on memories heavily rely on two types of memories: DRAM and Hard Disk Drives (HDDs). DRAM which is more expensive per gigabyte relies on the storage of charge in a capacitor to store information. This mechanism has fast access times, but it is a volatile memory. The charge in a capacitor leaks away after time and thus it requires refreshment cycles within a time window. Moreover, the data on DRAM is prone to get corrupted after reading the accessed data, thus the data has to be rewritten after each read. On the other hand, HDDs are cheap per gigabyte and are not volatile, thus their primary use is to store data. On the negative side, HDDs are composed of a reading-writing needles and rotating magnetic discs which are inherently slower. Moreover, power consumption, heat generated and large design make HDDs not the best option for portable devices. In recent years, reduction in cost of flash memories and a strong market for portable devices like smartphones and cameras have provided a fertile soil for production of Non-Volatile Memories (NVM).
1.2. Non-Volatile Memories

NVM has existed ever since the earliest 70s at which time Erasable Programmable Read Only Memories (EPROMS) were developed at Intel. EPROMs stored the data in a double gated transistor consisting of a control gate and a floating gate sandwiched between two insulators which are capable of storing charge (Figure 1) [1]. In this setup, a high voltage in the control gate produces an opposite charge in the floating gate, which at the time produces a channel in the transistor. Erasing or removing the charge of the floating gate requires a UV light as a source of high energy photons. The photons have the capacity of providing enough energy in the floating gate, so charges can move to the substrate as a parasitic current. [1]

Figure 1. Structure of a floating gate transistor showing (a) elements of the transistor structure and (b) circuit symbol.

The use of UV light to erase EPROM is not only inconvenient but also is also costly due to the need of a window in the package. Therefore, by making the top insulator thinner allows the creation of Electronic Erasable Programmable Read Only Memories (EEPROMs) that permit high voltages to introduce or remove charges from the floating gate. EPROMs and EEPROM were commonly used as firmware memory for embedded products and they were used frequently by design or development engineers to produce device prototypes [1].
1.3. Flash

Flash represents an important advance for NVMs, its proliferation, cost, capacity and form factor have made flash an important option as a storage solution in recent years. “Flash” memory borrows its name from developers who while using this type of memory found it be a “flash” time to erase and write on them compared to previous generations of NVM like EEPROMs [1].

Flash is already the mainstream memory for portable devices due to its form factor, low power consumption and media storage capacities. Besides, the proliferation of flash in embedded systems is also very dominant thanks to the advantage of its access speed, allowing developers to create prototypes faster, and the ability to support very easily products already in the market by upgrading the product’s software [1].

Stress on the devices from writing and reading causes wear and produces permanent damage that eventually renders them unusable. Two characteristics that are specific to NVMs and help to describe and compare the performance of a NVM are retention and endurance. Retention refers to the amount of time that a NVM in use will take to produce a corrupted value. In contrast, the number erase-write cycles that it takes to damage a device is called endurance and the minimum industry standard for NVM is 10000 cycles [1]

Flash can be found in two types: NOR and NAND memories having certain applications and advantages over each other depending on the application. Memory can be categorized by their use which can be code, data storage or the combination of both traits. Flash exists in two forms which emphasize code or data storages, and it is the historical successor for EEPROM technologies.

1.4. NOR Flash

NOR architectures are composed by transistors placed in parallel by word line, while the bit line is common to transistors in different word lines. This set up provides NOR its advantages: fast random access time and 100% reliability. NOR flash is suited for code execution, as well as for the combination of code and data. Code is benefited from NOR flash by a reliable storage, while NOR also provides fast
data access to branches and jumps required in the code. NOR is also suitable for applications where time is a constraint due to fast access times [1].

1.5. NAND FLASH

The second type of flash is NAND and, in contrast to NOR flash, the transistors are connected in a series fashion saving contact space and thus allowing denser IC utilization which makes it inexpensive compared to NOR flash. The series connection of NAND flash in bit lines takes a toll in the complexity required to read a bit. Complex circuitry and Error Correction Coding (ECC) need to be put in place, so the change in a bit line corresponds to the transistor selected by the word line, thus NAND does not provide 100% bit reliability. Dense memory and complex read mechanisms make NAND a suitable option for data storage (i.e. videos and music files) in which data is accessed sequentially [1].

This section compares different approaches that are being researched for future semiconductor memories. The two main components that will drive one of these technologies further into a widespread availability are economics and other characteristics that can outperform current technologies. The technologies reviewed in this section were selected based on their commercial and technological viability.
2. Future Generation Memories

2.1. Current Challenges

Memory has been the most aggressive market commodity in the semiconductor industry; the pursuit of higher profits makes the memory arena a rapidly evolving environment. Currently flash is the leader in NVM; however, it faces several challenges that predict the need for enhancement of present technologies or the adoption of different approaches. Major aspects of memories that will be required in the near future are continued scalability, lower voltage programming, faster programming speed, better endurance and better retention.

Scaling flash is threatened by the same means that allow non-volatility in flash: the insulating layers at the gate (Figure 1). In order to have enough energy to program the floating gate, a high enough voltage at the control gate needs to be applied to produce a strong charge at the floating gate. However, since the large voltage needed at the control gate creates constraints on the IC area, isolation needs to be kept constant to avoid the creation of parasitic currents in the form of hot carrier injection. Another factor that prevents scaling specifically of the channel is how the dominance of short channel effects as transistor shrink. At last, the transistor widths are determined according to specifics of the IC as well as isolation between devices which might be constrained in future generations [1].

At the same time, the charge at the floating gate should be kept at a desired variance of 20% for a time frame of ten years. This characteristic is known as retention which is defined as the amount of time between the writing of a value and the first erroneous readout [1]. This requirement puts a constraint on the perpendicular dimension of the transistor because leakage due to Fowler-Nordheim tunneling is present. In order to meet the retention requirements on flash, a floating gate with an approximate minimum gate of oxide thickness of 8nm is needed [1].

Another major drawback on flash technology is the programming time which goes from the tenths of microseconds up to a couple of milliseconds. DRAM, in contrast, has speeds close to 100ns and SRAM only needs a few nanoseconds [1]. The large times to write and erase in flash is due to the time required to inject and extract charges from the floating gate the conventional way of reducing this time is through erasing blocks at the same time.
Endurance is closely related to the failure rate of memories and is described as the number of read-write cycles that a memory can undertake before stress will cause the readout of a corrupt value or cause permanent cell damage. Stress during the read/write cycles will eventually cause a memory cell to lose its capacity to behave as memory. Endurance values of $10^5$ to $10^6$ are common for flash memories, as the device will eventually wear out due to deficiencies in the tunneling oxide [1].

### 2.2. NROM Memories

An option that has always been explored, just like in flash, is to improve on CMOS structures to create memories. One of these approaches is NROM. NROM is a NFET transistor that implements a stack of Oxide-Nitride-Oxide (ONO) dielectrics at the floating gate. An advantage that NROM offers is that there is a localization of charge which makes it immune to failures for one bit storage. NROM also has the capability of storing more than one bit in a cell by having a tight control of the output currents. This feature is known as Multi Level Cells (MLC), for which 2 and 4 bit MLCs have already been demonstrated [2][3].

The NROM basic structure is based on the CMOS device but instead of a gate, the NROM uses a trapping material stack. The stack used in NROMs is ONO where nitrogen acts as trapping material in between oxides of roughly 5nm to prevent leakage through tunneling (Figure 2). The use of an insulator as a gate improves on the concept of floating gate by localizing the trapped charge. In a floating gate structure, a point defect resulted in charge leakage and eventually the loss of all the charge due to the freedom of movement that charges have in a conductor. In contrast, a point defect on an insulator (in this case a nitride) only drains the charge directly on contact to the defect, this allows higher reliability. Endurance larger than $10^5$ has been already reported and retention values of $10^5$ has been achieved.
2.3. Ferroelectric Memories

Ferroelectric memories (FeRAM) have generated high expectations as they exhibit low power voltages, fast programming times and retention time above 10 years. Ferroelectric memories work by observing an extra charge generated by movement of an atom in the material crystal that is generated when the material is electrically excited. The major drawback for this type of memory is the high cost due to the need of using high permittivity materials such as Perovskite crystals and layered super lattice structures for the active layer [1]. Electrode compatibility to prevent hydrogen degradation is also a concern and the integration of these processes to standard silicon manufacturing has also created a burden on FRAM affordability [1]. Figure 3 depicts a cross section of a FRAM FET where the ferroelectric material is insulated from direct contact to silicon.
Ferroelectric memories exhibit voltage scaling as the dimensions do, the only constraint is that if faster programming speeds are needed; higher voltages might also be required. Although switching speeds of 1ns have been reported where considering only the ferroelectric memory, actual circuits have programming speed of 10ns [5],[1]. A major challenge on Ferroelectric memory speeds is the dependence on temperature; faster programming times are achieved at high temperatures. Lead Zirconate Titanate (PZT) and Strontium Bismuth Tantalate (SBT) have been characterized for endurance cycles above $10^{12}$ and data extrapolated for PZT indicates plausible endurances above $10^{16}$ [1]. PZT and SBT can be continuously scaled until the thinnest ferroelectric film is formed and, in contrast, the switched charge due to polarization will increase. However, SBT may be hindered due to the high annealing temperatures required at processing. Current ferroelectric memories are used in older processing technology nodes, but their cost is comparable to those found in NOR memories [1].

2.4. MAGNETIC MEMORIES

Resistance change is experienced in a Magnetic Random Access Memories (MRAM) by means of using parallel and anti-parallel magnetic fields. One example is the spin valve-type (Figure 4) based on Giant Magnetoresistance (GMR). In this image a layered system consisting of a two magnetic materials separated by a non-magnetic conductive layer composes the basic cell. A magnetic layer is
“pinned” using an antiferromagnetic layer that has a permanent magnetic field with momentum in one direction. The information is stored in the unpinned layer which can change magnetic momentum either parallel or anti-parallel with respect to the pinned layer [6],[7]. The non-magnetic conductive material sandwiched by the magnetic layers serves as the write and read mechanism. If a large current is applied to the conductive layer, the magnetic field of the unpinned can be changed effectively by writing a value to the cell. In the opposite scenario a small current is used to sense the magnetic field of the unpinned layer, if the current experiences high resistance an anti-parallel field is being stored which is caused due to large amount of electron scattering [6],[7].

![Diagram of a spin valve-type GMR MRAM](image.png)

**Figure 4. Structure of a spin valve-type GMR MRAM [7].**

Magnetic Tunnel Junction (MTJ) MRAM systems have a similar structure to the GMR cell described before, but instead of having a conductive layer sandwiched; a TMJ has a thin non-conductive material in between. In this system, writing operations, which changes the magnetic momentum, are performed by applying currents in the word line and column line. However, read operations are performed by allowing some current go through the MTJ structure. Again, low resistance and high resistances caused by the parallel or antiparallel field at the unpinned layer are interpreted as bits.
MRAM technology is very attractive due to some advantages that are conveyed by the ferromagnetic mechanisms. Since no structural wearing out is caused due to read-write operation in MRAMs, a theoretical infinite endurance is the theoretical maximum; endurances in the range of trillions have been already reported. MRAM retention is close to those found in flash and DRAM technologies. MRAM has one of the fastest programming speeds with times lower to 1ns. Dimension adjustments can be done like reducing the thickness of the junction proportional to the area of the MTJ cell, so resistance may be kept constant. Although current costs of MRAM is slightly higher compared with flash and DRAM, these costs can be brought down as MRAM become a mainstream technology [1][6].

2.5. PHASE CHANGE MEMORIES

Phase Change Memories (PCM) rely on a physical mechanism that, like its name describes, a phase change in the material produces a change in the electrical and optical properties. PCM materials that exhibit this behavior are chalcogenides with the main proliferation of systems based on Germanium Antimony Tellurium (GST) alloys. The phase change mechanisms in chalcogenides can be observed by applying energy, usually light or electricity, to change the material from a polycrystalline state to an
amorphous state. When energy is applied the material, the same is heated and if a temperature above the melting point is reached, an amorphous state is obtained. The low resistance state is accomplished by either heating the chalcogenide just below the melting point or by slowly cooling down the material [1],[6].

The basic structure of a PCM cell can be observed in Figure 6, it is electrically depicted as a conjunction of resistors connected in series. In this cell, a current is forced through the top electrode, which at the same time activates the heater and thus produces a phase change for programming operations [1]. Reading operations are performed by simply allowing a small current (that does not change the phase) through the cell.

![Figure 6. Basic structure of a PCM cell [1].](image)

Studies in PCM have shown that this mechanism has an excellent retention of above ten years, which if data is extrapolated is estimated to reach up to 30 years. Since phase change is a mechanism not based on charge, PCM offers immunity to radiation. PCM scaling might pose a problem, as technology nodes are shrunk, enough current to heat activate the phase change might not be reached. Besides, there has been also a concern that thermal cross-talk might affect future generations of PCM [1]. Consequently, dimension tuning of PCM is critical, so resistances and thermal coefficients can be kept constant.

**2.6. SUMMARY**

NROM and other forms of ONO based memories that now include a high-k dielectric in their stack are a current mainstream technology for flash that is expected to serve as a bridge technology for other types of memory. FRAM has already been commonly included as embedded memory, even though
integration with silicon is still challenging. MRAM offers very high reliability although the industry
does not seem ready to fully adopt this technology. PCM’s small crossbar architecture, radiation
hardness, and high reliability have allowed it to appear as a standalone offering by a couple of
companies.

As flash technology begins to falter as a viable solution, the proliferation of the technologies
mentioned above will increase. Finally, the emphasis of this thesis is on memristors, which will breed
yet another type of memories called Resistive Random Access Memory (RRAM). RRAM is still a
laboratory device that is expected to move fast from a prototype phase to its first commercial
breakthrough. Memristor, the single cell of a RRAM, will be discussed in further consideration in the
following sections.

3.1. Prediction and Theory of the Memristor

Conventional electric circuits are defined by the combination of four electrical variables: voltage \((v)\), current \((i)\), charge \((q)\) and magnetic flux \((\phi)\). As such, there a total of 6 possible combinations as described by Equations 1 to 6. Charge is described by the time integral of current and has units of coulombs.

\[
q(t) = \int_{t_0}^{t} i(\tau) d\tau \quad \text{Eqn. 1}
\]

Subsequently, a time integral of voltage is the definition of magnetic flux \((\text{Wb})\)

\[
\phi(t) = \int_{t_0}^{t} v(\tau) d\tau \quad \text{Eqn. 2}
\]

The last four equations describe the fourth passive electrical devices starting with resistance \((\Omega)\) conveyed by the first derivative of voltage with respect to current.

\[
R = \frac{\partial v}{\partial i} \quad \text{Eqn. 3}
\]

Capacitance \((\text{F})\), an energy storing device is defined by deriving charge with respect to voltage.

\[
C = \frac{\partial q}{\partial v} \quad \text{Eqn. 4}
\]

The second energy storing device is the inductor \((\text{H})\) and it is defined as the change of magnetic flux with respect to current.

\[
L = \frac{\partial \phi}{\partial i} \quad \text{Eqn. 5}
\]

The last and unnoticed fourth passive device is the memristance \((\text{Wb/C})\), obtained by the first derivative of magnetic flux with respect to charge.

\[
M = \frac{\partial \phi}{\partial q} \quad \text{Eqn. 6}
\]

Interestingly equations 3, 4 and 5 define the well-known passive devices; resistor, capacitor and inductor, respectively. In 1970, Leon Chua predicted, based on Equation 6, which describes the
relationship between $\varphi$ and $q$, that a fourth passive device should exist [8]. Chua named the relationship “memristance” because their time varying relationship makes this device behave like a resistor with memory [8],[9].

An interesting and highly useful feature of memristance is that its value can change with respect to time, a feature that made it hard to find. A memristor that has a single valued function (i.e, $\varphi=\varphi(q)$) is said to be a charge controlled or magnetic flux controlled. For instance a charge controlled memristor, as indicated in Eqn. 6, will depend on the charge that has flowed through it in the past.

the memristor reduces to a resistor with constant $R$ in case that the relationship between charge and magnetic flux is linear [8].

Memristance can be implemented by the use of circuitry, however in order for a memristor to be considered a passive device it must obey four theorems proposed by Chua. The first theorem, the passivity criterion indicates that a memristor must have a positive value of resistance, in other words, power, $p > 0$ as calculated in

$$p = i(t)v(t) = M(q(t))[i(t)^2]$$

Eqn. 7

The voltage versus current behavior of memristors has a pinched hysteresis pattern as shown in Figure 7. This leads to the second theorem related to the pinched hysteresis. A couple of two (at different states) IV curves must form an origin crossing pinched hysteresis. An interesting phenomenon in the memristors is that its instantaneous value (resistance) tends to converge in a sole value as frequency increases (Figure 8) [9]. A behavior that can be explained mathematically by

$$\varphi(t) = \varphi_0 + \int_{t_0}^t A\sin(\omega\tau)d\tau = \varphi_0 + \frac{A}{\omega}\cos(\omega\tau) \to \varphi_0, as \ \omega \to \infty$$

Eqn. 8

This equation shows the convergence of a sinusoid input to a memristor (in this case flux) as frequency goes to infinity. Physically, the memristor shows some inertia to motion and thus it cannot adapt to a different value at fast enough frequencies. Since, the hysteresis is restricted to be positive and confined to always cross the origin, it is a characteristic that yields the third theorem: passivity condition. Unlike the capacitor or inductor that can store energy, the origin crossing trait of the memristor provides that it has to be a non-energy device in analogy to a resistor [9].

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The last and fourth theorem applies for the charge-controlled and flux controlled memristors. This theorem provides that the relationship between charge and flux has to be an increasing monotone function. The reasoning for this theorem is that for the case that a nonmonotonic function is used to express the charge or flux controlled expression, there must be a negative point in the curve that at the same time yields a negative point in the slope. Consequently, in this case the memristance $M$ is negative, hence it violates the first theorem (passivity).

Figure 7. Characteristic hysteresis pattern of a memristor [9].

Figure 8. Characteristic hysteresis pattern showing a decrease in the enclosed area as the frequency increases [9].
3.2. RESISTIVE SWITCHING MECHANISMS

Memristors in general have a structure known as MIM or Metal-Insulator-Metal, where the metal can be interchanged for any good electron conductor and common insulators are binary oxides, multinary oxides, as well as chalcogenides [10]. Memristors need a high electric field (implemented by applying a voltage between the electrodes) to create a conduction path in the insulator layer. Resistance switching in a memristor is achieved by applying a threshold voltage (set voltage) which forces the memristor to go from a high resistance state (HRS) to a low resistance state (LRS). Subsequently, a switch from LRS to HRS occurs when a large current goes through the device. Two types electrical behaviors are observed in memristors: unipolar and bipolar (Figure 10). Unipolar behavior occurs when the switching mechanisms, HRS-to-LRS and LRS-to-HRS, are independent of voltage and current polarity. In contrast, bipolar behavior occurs when the device needs to be driven to one polarity to go from HRS to LRS; while driving the device in the opposite polarity is needed to reset the memristor to HRS.

3.2.1. Homogeneous Theory

In 2008 S. Williams, head of HP’s R&D Division in Palo Alto, California reported that the resistive switching demonstrated by metal-insulator-metal devices, they were developing satisfied the properties of a memristive system predicted by Chua [11]. The report entitled “The missing memristor found” conveyed not only the Pt/TiO₂/Pt system as a memristor, but it also proposed a mechanism for the resistive switching. (It is worth noting however that the originally proposed mechanism based on a moving boundary was later debunked and replaced by the filament mechanism.)

MO memristor is modeled by considering a semiconductor divided in two parts which effectively behaves as two resistors connected in series (Figure 9). The undoped part of the semiconductor has high resistance, while the doped part of the semiconductor exhibits low resistance. Williams considered the thickness of the film, ion mobility, low and high resistance and charge for his model.
3.2.2. Filamentary Theory

The conduction mechanism in MIM has been reported to be a localized filamentary phenomenon rather than a homogeneous effect. Figure 11 depicts the filamentary nature of MIM memristor system where a stacked or a vertical contact can be observed along with its lateral counterpart. This mechanism consists in applying a voltage (current limited) between both electrodes of the memristor, at which time a partial electrical breakdown of the insulating layer occurs and a filament is formed. The filament might be composed of the metal material, residual carbon or by a reduction of the insulating material [12]. Once the filament has been created, large current through the filament causes high joule heating densities in a very small area, thus the filament melts down leading back to an HRS state [12]. MIM structures in high electric fields can experience Fowler-Nordheim tunneling and with conjunction of charge traps due to defects or metal nanoparticles, charges can be injected to the insulator. There is also indication that electrostatic in the insulating layer or charges behaving as dopants may be responsible for lowering the resistance in some memristor systems [12].
4. Survey of Memristor Device Approaches

4.1. Development of TiO2

In order to further understand the mechanism for resistive switching, HP has created a device consisting of a titanium top electrode, an insulating layer of titanium oxide and a bottom electrode of platinum (Figure 12). Ion movement in the Pt/TiO2 interface due to the applied electric field is
identified as the major means to shunt or short circuit the electronic barrier between the metal and the insulating layer. One significant advantage of metal oxides as insulator versus other approaches like perovskite crystals is the ease of fabricating and doping the titanium oxide layer with standard CMOS tools [14].

Figure 12. Cross-sectional TEM image of a Pt/TiO2/PT memristor [15].

HP obtained experimental data of fifty switches and compared it to a rectifying memristor circuit (Figure 13). As it can be observed in Figure 13, the experimental data of titanium dioxide is matched theoretically by connecting a rectifying diode in parallel with a memristor. Analysis of the IV behavior indicated a Schottky behavior for the top electrode (TE) and Ohmic behavior for the bottom electrode (BE) [9].
At the end of the year 2008, HP introduced the use of memristors in logic circuits. A defect tolerant memory array in a 2D configuration was reported with scalability down to the molecular level [16] [17]. Some of the advantages that this structure can offer are lower power consumption, higher clock frequencies and better use of silicon real estate when used for FPGA development [16]. For instance, Figure 14 shows an optical and an SEM image of the hybrid system with the nanomemristor array in the middle and the transistor logic at the edge of the array. Lastly, HP has made significant advances in the use of titanium dioxide memristors beyond a memory cells by implementing logic and latches with memristors [17][18][19].
4.2. Silicon in Memristive Systems

The introduction of new materials to integrated circuits is avoided by the semiconductor industry due to concerns of high development costs and potential reliability issues. Therefore, the continued use of silicon is something that is looked after by the industry in all technologies, including memristors. Silicon oxides are easily created with standard CMOS tools and fortunately the memristive behavior is observed in this material.

One of the earliest documents on silicon oxide based memristors is “Unipolar resistive switch based on silicon monoxide realized by CMOS technology [20].” In this paper, the authors describe the fabrication of a W/SiO/Cu (Figure 15) resistive switching stack. An important feature of this device is the deposition of the silicon monoxide by PECVD with process temperature of 300°C. The low temperature process is an important feature that allows the use of this technology with 3D stackable devices [20].
This system has shown a unipolar behavior with an HRS/LRS ratio of $10^4$ and retention up to 5000 cycles. The conduction mechanism of the device (Figure 16) has been described to match the Frenkel-Poole model [20]. Physically the conduction mechanism can be related to the displacement and charge trap of copper ions into the deliberately porous silicon monoxide. It was observed in endurance tests (Figure 17) that the HRS of the device might be affected by the diffusion of copper. During the first write-read cycles the HRS depicts a very high resistance ($\sim 10^9 \, \Omega$), but as the device is being switched more copper ions diffuse. Once the diffusion of copper has been saturated, a lower resistance for the HRS state is established ($\sim 10^6 \, \Omega$) [16].
Figure 17. Endurance of the W/SiO/Cu memristor [20].

Another silicon oxided-based memristor that has been studied is composed of p-Si/SiO$_x$/p-Si (Figure 18). These devices show unipolar behavior with a large HRS/LRS ratio of $10^5$ and write times less than 100ns [21]. An important finding in this article is the formation of the filament to create the conduction path. The authors created a CNT/ SiO$_x$/CNT structure which was cut by focused ion beam after the formation of the conduction path. Figure 19 shows a TEM image of the conduction path where the alignment of Si nano-cubes (NC) with on percolation path parallel to the current direction [21]. In order to totally eliminate the possibility of metal electrode diffusion as the conduction mechanism on the SiO$_x$, the authors used Ti, W, Sn, and carbon nano-tubes (CNT) and no important difference was found on the conduction behaviors of the system [21].

Figure 18. (a) Schematic drawings and (b) SEM image and top-view drawing of a p-Si/SiO$_x$/p-Si memristor structure [21].
A highly integrated crossbar array based on silicon has been presented by the University of Michigan, in which a 1 kb ReRAM was presented. The MIM system is composed by a p-Si/ a-Si/ Ag (Figure 20) obtaining a set/reset ratio of $10^3$ and writing pulses of 10 ns for a 120 nm$^2$ active areas [22]. An important feature of this mechanism is that HRS can be tuned from 10 KΩ to 100 MΩ by changing the amorphous silicon deposition parameters. In order to reduce the series resistance due to the p-Si, electrodes of Ni were also implemented [22].

The endurance of this device was drastically affected due to high currents up to 1 mA that could affect the integrity of the device. The system is thus proposed as a write-once read-many times memory device. The possible explanation for the high currents experience with nickel is that the metal electrode/ a-Si interfaces produce higher number of traps which at the same time allow creating more metallic filaments in the amorphous silicon [22].
4.3. MEMRISTORS ON FLEXIBLE SUBSTRATES

An area that has generated much of interest is flexible electronics due to the versatile forms and robustness that can be offered by this option. Presently there are a few reports of memristors on flexible substrates; however they indicate the potential of incorporating memristors into flexible electronics.

4.3.1. Organic Memristors on Conductive Polypyrrole Film

Memristors made of organic materials for the active layer have been demonstrated on flexible substrates and accentuate the intrinsic advantages of both memristor devices and organic electronics like low cost, 3D stacking and scalability. One approach is to use a conjugated copolymer of 9, 9-dihexyfluorene and benzoate with chelated europium tnehoyltrifluoroacetone ligand complex (F6FBEu) on a flexible and conducting polypyrrole (PPy) substrate. The polypyrrole substrate serves as the BE and gold serves as the TE as shown in Figure 21 [23]. The thickness of the F6FBEu layer is ~50nm. The PPy and gold thicknesses are ~40µm and 0.2µm, respectively. The smallest devices have a contact area of 150 µm². This organic flexible memristor exhibited a set/reset resistance ratio of 200 and an endurance of 10⁶, however one major drawback is that it is a write only-once and read many-times device.
Figure 21. Diagram of a PPy/P6FBEu/ Au memristive device [23].

4.3.2. **Flexible Spin-Coated TiO$_2$ Memristors**

Flexible memristors have been demonstrated using an Al/TiO$_2$/Al stack on transparency film as shown in Figure 22[24]. In these devices the TiO$_2$ layer is created by spin coating a titanium isopropoxide sol-gel. The sol-gel is spun coated and then air dried to obtain a 60 nm film. The top and bottom electrodes are deposited by thermal evaporation giving a thickness of 80nm.

The electrical characterization of the device revealed a bipolar behavior with a set switch voltage of 4V and a reset voltage of -2V as shown in Figure 23. Retention of $1.2 \times 10^6$ seconds (14 days) was demonstrated. Interestingly, the memristor was flexed 4000 times and an HRS/LRS resistance ratio of $10^4$ was maintained indicating its applicability as a flexible memory device.
4.3.3. **Graphene Oxide Memristors on PES**

Spin coating is an approach that was also used in the creation of graphene oxide (GO) memristors. These memristor devices were fabricated on polyethersulfone (PES) substrates. Aluminum top and bottom electrodes were deposited by thermal evaporation. The thickness obtained for the stack Al/GO/Al corresponds to 70nm for the electrodes and 15nm for the GO as shown in Figure 24[25].

This system has a bipolar behavior with an HRS/LRS ratio of 100, retention of $10^5$ s and endurance of 100 cycles. The conduction mechanism for the GO flexible memristor has been proposed to be governed by filamentary formation showing a space-charge-limited-conduction behavior [25].
4.3.4. ZnO Memristors on Stainless Steel

A memristor system of ZnO on stainless steel has been fabricated in Korea using CMP polished stainless steel sheet serving both as the substrate and as the BE [26]. As shown in Figure 25 the ZnO layer was deposited with RF sputtering, while the gold Top Electrode TE was deposited by means of thermal evaporation. Thickness of the ZnO functional layers are 20 nm to 40 nm. The ZnO memristor demonstrated both unipolar and bipolar behavior with typical set voltages of 1.2V and reset voltages of 0.6V. The LRS state shows an Ohmic conducting mechanism while the HRS is governed by Frenkel-Poole conduction [26].

Figure 25. ZnO memristor on a stainless steel substrate [26].

4.3.5. Transparent ZnO Memristors on PES

Another work from Korea explains a very interesting flexible and also transparent memristor device using ZnO. The structure starts on a polyethersulfone substrate where a 40nm/20nm/40nm ITO/Ag/ITO stack is chosen as the BE due to its high sheet conductance and high optical transparency properties [27]. An insulating ZnO of 50 nm is then deposited by RF sputtering. The TE is ITO deposited via pulsed laser deposition. The device demonstrates unipolar behavior with 0.6 V and 1.5 V for reset and set voltages, respectively. The conduction mechanisms dominating the IV behavior of the memristor are Ohmic and HRS at high voltages above 1V behave in accordance to the space-charge-limited-current (SCLC) mechanism[27].
Figure 26. Transparent ZnO memristor on polyethersulfone substrate [27].

4.4. SnO$_2$-Based Memristive Systems

SnO$_2$ is an n-type semiconductor with a band gap of 3.5 eV and although it demonstrates a wide resistivity range, it has not received much attention. The first reported SnO$_2$-based memristor was by a research group in Japan which used low temperature pulsed laser deposition of SnO$_2$ that is compatible with CMOS fabrication [28]. In this work, Pt, Ti, and Au were tested and compared as contact electrodes. The SnO$_2$ layer was 40 nm thick as shown in Figure 27 which provides a cross sectional view of the memristor with Pt electrodes. Electrically, the SnO$_2$ memristor demonstrated unipolar behavior with set voltages between 1.5V and 2V and reset voltages ranging from 0.5V to 1V (Figure 28). Endurances of 100 cycles and retention of $10^4$ seconds were demonstrated [28].
Figure 27. Cross-sectional TEM image of a Pt/ SnO$_2$/Pt memristor system [28].

Figure 28. IV characteristics of a Pt/ SnO$_2$/Pt memristor system [28].

The memristors demonstrated Ohmic transport in LRS with Au, Ti and Pt electrodes as shown in Figure 29 (a) and the conduction mechanism was attributed to oxygen vacancies allowing the formation of a Sn rich filament. In HRS, Ohmic behavior was observed only for the Au and Ti electrodes as shown in Figure 29 (b). In contrast, the Pt electrodes exhibited a Schottky behavior at low electric fields and Poole-Frenkel at high electric fields as shown in Figure 29 (c) and Figure 29 (d), respectively [28].
Figure 29. IV characteristics of the SnO$_2$-based memristor showing (a) Ohmic behavior in LRS and (b) Ohmic behavior in HRS only for Au, Ti while Pt deviated from Ohmic. The Pt electrode showed (c) Schottky emission at low electric fields and (d) Poole-Frenkel conduction at high electric fields [28].

A second SnO$_2$ based memristor was reported by University of Texas at El Paso (UTEP) researchers in which the stack is composed of Ti/SnO$_2$/Ag (Figure 30) on glass substrates. The BE and insulating layers are deposited with RF magnetron sputtering. The uniqueness of this work is the implementation of silver ink as the TE. The dimensions of the critical SnO$_2$ insulating layer reported by this document are 45 to 53 nm. A unipolar behavior with reset and set voltages of 0.8 and 1.2 V was reported, as shown in Figure 31. Although the group from Japan reported the conduction mechanism with Ti contacts, Almeida was the first to report the conduction mechanism for SnO$_2$ using Ag contacts. An Ohmic behavior for LRS and HRS was the conduction mechanism for both cases. Nevertheless, no model fitted the conduction behavior of HRS above 0.3V and it is suspected that this was due to the time variant nature of the memristor when undergoing switching from HRS to LRS. [29].
Figure 30. Cross-sectional SEM image of the Ti/SnO₂/Ag memristor [29].

Figure 31. IV Characteristics of the Ti/SnO₂/Ag memristor [29].
Figure 32. HRS conduction process analysis showing Ohmic conduction below .05 MV/cm and deviation above 0.05 MV/cm. [29].
5. Memristor Fabrication

5.1. Introduction

This chapter discusses the fabrication of MOM Ti/SnO$_2$/Ag memristors on glass and plastic substrates. The Ti and SnO$_2$ layers were deposited using RF magnetron sputtering under different conditions. The top contacts were created using silver paint by hand.

5.2. Surface Preparation

The surface preparation used for the glass slides and Kapton plastic substrates differed due to chemical compatibility and the conditions of the material. Figure 33 depicts the cleaning procedure that was followed for both glass and Kapton substrates. The microscope slides were pre-cleaned by the manufacturer thus little contaminants were on the surface. In contrast, the 2”x2” Kapton substrates contained a significant amount of dust which may have been the cause of scratches on the surface.

In order to remove the dust, the Kapton films were initially dipped in methanol, rinsed in DI water, and then dipped in a basic solution. This solution was composed by five parts of DI warm water (60°C), one part of hydrogen peroxide and one part of ammonium hydroxide. The solution removes organics and metals and performs a mild etch on the Kapton that further promotes the cleaning of the surface. The solution chosen for cleaning the glass slides was a combination of sulfuric acid and hydrogen peroxide with a ratio of 3 to 1. This acidic solution is capable of removing most organics and also etches mildly the surface of the glass. Finally, both the glass and Kapton substrates were thoroughly rinsed in DI water, nitrogen dried and baked to remove moisture.
Figure 33. Cleaning procedure for (a) glass (b) Kapton.

5.3. TITANIUM DEPOSITION.

A planar thin film deposition was performed using a 2” diameter target and a square substrate area with dimensions 2”x2”. The conditions to deposit titanium were emulated from the work done by S. Almeida [29]. Figure 34 summarizes the Titanium deposition conditions that provided a reliable bottom electrode. Electrical conductance and smoothness are important parameters for the BE, hence the Ti layer has to be sufficiently thick and smooth. Low pressure (<1.2mTorr) is kept during deposition to
promote a high deposition rate (10nm/min). Also, titanium storage in a desiccator is highly advised, since an oxygen layer can be formed on the target (and therefore transferred to the substrate) if kept in air. Titanium conditions for both Kapton and glass were same and the Figure 35 shows photographs of the titanium layer on the substrates.

Figure 34. Titanium deposition parameters.

Figure 35. Titanium films on (a) glass and (b) Kapton substrates.
5.4. Tin Dioxide Deposition

Tin dioxide deposition was performed immediately after the titanium deposition to avoid contamination of the film. A metal shadow was used to define the area where SnO$_2$ was deposited as shown in Figure 36. 100% partial pressure of oxygen was used to deposit fully oxidize tin dioxide based on the work of S. Almeida [29]. The parameters were optimized for the work in this thesis and are shown in Figure 37. A good memristive behavior is highly dependent on the thickness of the tin dioxide layer, thus it is important to tightly control this parameter. Although deposition thicknesses of 26 nm and 29 nm are reported for Kapton and glass, memristors with tin dioxide thicknesses of 20 nm to 40 nm were created.

![Figure 36. Tin dioxide /Titanium films on (a) glass and (b) Kapton substrates.](image)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Base Pressure</td>
<td>10^{-6} Torr</td>
</tr>
<tr>
<td>Ox Flow</td>
<td>82 sccm</td>
</tr>
<tr>
<td>Forward Power</td>
<td>40 W</td>
</tr>
<tr>
<td>Deposition Pressure</td>
<td>5 mTorr</td>
</tr>
<tr>
<td>DC power</td>
<td>-124 W</td>
</tr>
<tr>
<td>Time</td>
<td>26 min</td>
</tr>
</tbody>
</table>
Figure 37. Tin dioxide deposition parameters.

### 5.5. Silver Application

One of the most remarkable findings of Almeida’s work was the use of silver ink as the top electrode for the first time [29]. Almeida applied EMS 18DB70X silver conductive paste with highly accurate volumetric pipettes (Figure 38) and hand applied with a brush. In this work only hand applied contacts were studied and the finished devices on Kapton and glass are depicted in Figure 39.

![Figure 38. Silver contact applied using a volumetric pipette.](image)

Figure 38. Silver contact applied using a volumetric pipette.

![Figure 39. Finished (a) glass and (b) Kapton Ti/SnO₂/Ag memristors.](image)

Figure 39. Finished (a) glass and (b) Kapton Ti/SnO₂/Ag memristors.
6. Electrical Characterization

6.1. INTRODUCTION

Characterization of the memristors was performed using a Nikon micromanipulator and the data was collected using LabView software to control a computer and a Keithley 2400 power supply. Voltage and current characteristics of the tin dioxide memristors were obtained by driving a positive voltage to the silver top electrode (TE), while ground was connected to the titanium bottom electrode (BE) as shown in Figure 40.

![Figure 40. Setup for electrical characterization.](image)

6.2. MEMRISTOR IV BEHAVIOR

The electrical behavior of a memristor shows three distinct stages or states; the forming stage, LRS and HRS. Figure 41 and Figure 42 show IV curves of the memristors fabricated on glass and Kapton substrates, respectively. The devices were switched 70 times (35 cycles) and exhibited unipolar behavior. The forming, LRS and HRS states are clearly observed and indicated by green, red, and blue traces, respectively.

The forming stage of a memristor is when it is switched from its initial virgin state to LRS. When the voltage (and therefore the electrical field) is high enough, a conduction path is created between the TE and BE and the device is then switched to LRS (red traces). It is believed that the conduction path is due to oxygen vacancies which produce a conductive Sn-rich percolation path for
charge flow. In order to avoid permanent damage, the power supply was current limited to 10 mA when the memristor was switched from forming (and HRS) to LRS. In order to switch the device from LRS to HRS, this time the memristor is driven to a strong current (~12 mA) to rupture the conduction path (blue traces). Subsequently, the memristor can be switched to LRS by applying a strong electric field to repair rupture in the conduction path. In this way, switching between LRS and HRS states is repeated achieved.

![Memristor on Glass](image)

Figure 41. IV switching characteristics of a memristor on glass. The memristor was switched 70 times.
Figure 42. IV switching characteristics of a memristor on Kapton. The memristor was switched 70 times.

6.3. ENDURANCE

Figure 43 and Figure 45 are endurance plots for devices on glass and Kapton, respectively. Although both devices have very stable LRS through all the plotted cycles, HRS for glass was lower after cycle 22. Figure 44 and Figure 46 show the cumulative percentage distribution of the memory endurance. It is observed that the resistance averages in HRS are similar for both Kapton and glass, whereas the mean in LRS is larger for Kapton. A statistical analysis reveals resistance switching ratios of 15 for glass and 10 for Kapton (see Table 1)
Figure 43. Memory endurance for a memristor on glass.

Figure 44. Distribution of the resistances in (a) LRS and (b) HRS for a memristor on glass.
Figure 45. Memory endurance for the memristor on Kapton.

Figure 46. Distribution of the resistances in (a) LRS and (b) HRS for a memristor on Kapton.
Table 1. Memristor endurance Statistical analysis.

<table>
<thead>
<tr>
<th>Endurance Statistical Analysis</th>
<th>Glass</th>
<th>Kapton</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>HRS</td>
<td>LRS</td>
</tr>
<tr>
<td>Min</td>
<td>171.16 Ω</td>
<td>38.85 Ω</td>
</tr>
<tr>
<td>Max</td>
<td>1507.6 Ω</td>
<td>116.82 Ω</td>
</tr>
<tr>
<td>Mean</td>
<td>713.48 Ω</td>
<td>46.26 Ω</td>
</tr>
<tr>
<td>Median</td>
<td>635.43 Ω</td>
<td>43.62 Ω</td>
</tr>
<tr>
<td>Variance</td>
<td>1.42x10^4</td>
<td>170.55</td>
</tr>
<tr>
<td>SD</td>
<td>376.74 Ω</td>
<td>13.05 Ω</td>
</tr>
</tbody>
</table>

**6.4. Set and Reset Voltages**

Figure 47 and Figure 49 are set and reset voltage plots for devices on glass and Kapton, respectively. Figure 48 and Figure 50 show distributions of reset and set voltages for memristor fabricated on Kapton and glass substrates, respectively. Statistical analysis of these data is provided in Table 2.
Figure 47. Set and Reset Voltage for memristor on Glass.

Figure 48. Distribution of (a) reset and (b) set voltages for a memristor on glass.
Figure 49. Set and reset voltage for a memristor on Kapton.

Figure 50. Distribution of (a) reset and (b) set voltages for a memristor on Kapton.
Table 2. Set and reset voltage statistical analysis for memristors.

<table>
<thead>
<tr>
<th>Set and Reset Voltage Statistical Analysis</th>
<th>Glass</th>
<th>Kapton</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min</td>
<td>0.788V</td>
<td>0.233V</td>
</tr>
<tr>
<td></td>
<td>0.947V</td>
<td>0.259V</td>
</tr>
<tr>
<td>Max</td>
<td>1.475V</td>
<td>0.889V</td>
</tr>
<tr>
<td></td>
<td>1.919V</td>
<td>0.956V</td>
</tr>
<tr>
<td>Mean</td>
<td>1.112V</td>
<td>0.485V</td>
</tr>
<tr>
<td></td>
<td>1.299V</td>
<td>0.259V</td>
</tr>
<tr>
<td>Median</td>
<td>1.131V</td>
<td>0.474V</td>
</tr>
<tr>
<td></td>
<td>1.309V</td>
<td>0.624V</td>
</tr>
<tr>
<td>Variance</td>
<td>0.0227</td>
<td>0.0103</td>
</tr>
<tr>
<td></td>
<td>0.0426</td>
<td>0.0247</td>
</tr>
<tr>
<td>SD</td>
<td>0.151V</td>
<td>0.102V</td>
</tr>
<tr>
<td></td>
<td>0.206V</td>
<td>0.157V</td>
</tr>
</tbody>
</table>

6.5. RETENTION

Figure 51 and Figure 52 are retention plots for devices on glass and Kapton, respectively. Since the current electrical characterization setup is manual, it was decided to obtain a plot every 5 min (300s) for 1:30 hrs. (5400s); then the state was switched from LRS to HRS to obtain the same amount of readings at this state. Retention was measured using 0.2V which is just below the minimum reset voltage reported by endurance. It was observed that there was a tendency of increasing resistance as cycles increased in HRS. The LRS values show a much smaller deviation; maximum-to-minimum differences of less than an 8 Ω and 2 Ω were observed for Kapton and glass, respectively. Resistance switching ratios of 77 and 29 were calculated for the memristors on glass and Kapton, respectively.
Figure 51. Retention for memristor on Glass.

Figure 52. Retention for memristor on Kapton.
6.6. RETENTION DEGRADATION.

Degradation of retention was observed when 0.3 V were used to read the resistance values as shown in Figure 53 for HRS and Figure 54 for LRS. These results show the importance of keeping the reading voltage below a certain level (~0.25 V) to ensure good retention and avoid switching.

Figure 53. Switch high to low while reading retention.
Figure 54. Switch low to high while reading retention.
7. **Structural Analysis**

7.1. **Surface Imaging**

Images of tin dioxide were obtained using a Hitachi S-4800 SEM and a Leica DMLM optical microscope to observe the morphology of the films. Figure 55 and Figure 56 depict the SnO$_2$ surface in which the contrast of the films deposited in glass versus Kapton is evident. While the surface of the tin dioxide on glass was relatively smooth with a few scratches (Figure 55), much more scratches and a rough surface were found on the tin dioxide over Kapton (Figure 56). The rough surface in Kapton is attributed to dust-induced scratches on the film. Scratches on Kapton were even evidenced by the naked eye, but an extreme scenario can be observed in Figure 57, an optical image of the tin dioxide surface with a 1000x augment. It is important to note that the images are different magnification and this needs to be taken into account for a more quantitative analysis of scratch density between the glass and Kapton substrates. Notwithstanding of the surface differences between the Kapton and glass devices, it is remarkable that even though a slightly lower yield was obtained for Kapton, both substrates gave in positive results.

Figure 55. SEM Image of tin dioxide over titanium surface on glass.
Figure 56. SEM image of tin dioxide over titanium surface on Kapton.

Figure 57. Optical image of tin dioxide over titanium surface on Kapton at 100X magnification.

An SEM image of a silver TE on a Kapton device can be observed in Figure 58; precipitates of silver ink can be observed. The contacts reported in this work had diameters of ~1mm to ~3mm due to application of silver by hand. One important advantage that silver ink as TE offers is the ease of removing the contact with little to no damage to the tin dioxide film by using acetone.
Figure 58. SEM image of a hand applied silver contact on tin dioxide.

7.2. COMPOSITION ANALYSIS

In order to know what composition the deposited Ti and SnO$_2$ films have, it was decided to use a Bruker Discover D8 XRD. Since the films were known to have dimensions in the nanoscale range, grazing incidence XRD readings for a time period of 2 hours were performed (Figure 59 and Figure 60). Although the counts are not as strong as it would be preferred, polycrystalline phases of SnO$_2$ and Ti were found by this method, especially on samples with glass substrate. Slight shift of the spectrum on Kapton compared to the database peaks can be observed in Figure 60 and this effect is attributed to strain experienced by the sputtered film due to bending of the Kapton. Moreover the peaks were much weaker for Ti and not observable for SnO$_2$ which could be attributed to bending and plastic structure of the Kapton film.
Figure 59. Grazing incidence x-ray diffraction pattern of SnO$_2$/Ti on glass.

Figure 60. Grazing incidence x-ray diffraction pattern of SnO$_2$/Ti on Kapton.
7.3. Thickness Film Measurements

A profiler was used to measure the thickness of the silver TE. Figure 61 shows a typical measurement for a memristor on glass and indicates a thickness of 5 μm.

![Graph showing thickness measurement](image)

Figure 61. Step height analysis performed with a profiler for Ag TE.

Thickness measurements for SnO₂ were obtained using specular reflectance with a Filmetrics F-20. Using this method, thicknesses of 26.86 nm and 29.28 nm were obtained for glass and Kapton respectively (Figure 62). This same method was also used to measure titanium which yielded dimensions of 220.3nm on Kapton and 198.6 nm on glass.
Figure 62. Thickness of SnO$_2$ by specular reflectance for a memristor on glass.

The values obtained by specular reflectance were confirmed using cross-sectional SEM of a memristor on glass. Figure 63 shows the cross section of a memristor with no Ag TE contact. It can be observed that the films measured 24.4 nm for tin dioxide and 182.6 nm for titanium. Thickness percentage discrepancies between the two methods used are 8.8% for titanium and 7.4% for tin dioxide.
Figure 63. Cross sectional SEM image of SnO$_2$/Ti on glass.

Controlling the SnO$_2$ thickness within ~20 nm to ~40 nm is important to observe resistive switching. If the thickness is too large or too thin, the device will not switch properly or at all. Therefore, a common practice to calibrate the RF sputtering reactive deposition of tin oxide is to deposit an umbrella of thicknesses. In this case, five deposition times ranging from 22 min to 30 min were used. The thicknesses of these depositions were collected using the Filmetrics F-20 and they are reported in Figure 64. Although all of the devices in this range work, it is speculated that the devices will not function if the thicknesses are outside this range.
Figure 64. Thickness profile of SnO$_2$ depositions.
8. Optical Characterization of SnO₂

8.1. Transmission and Reflectance

Using the Varian Cary 5000, specular, diffusive, total reflectance and total transmission were obtained for SnO₂. Tin dioxide was sputtered on sapphire to obtain clearer measurements by eliminating optical interaction with titanium. Figure 65 shows total transmission and reflectance for tin dioxide on sapphire.

![Tin Dioxide Absolute reflection and Transmission](image)

Figure 65. Total transmission and reflectance of tin dioxide on sapphire.

8.2. Refractive and Extinction Indexes

Using the Filmetrics F-20, as shown in Figure 66, the thickness of the tin dioxide film was determined to be 41.51 nm with a goodness of fit of 0.9994. This analysis also outputs the refractive index coefficients for the fitted spectrum. Lambert’s Law describes the relationship between transmission, absorption and thickness [30] and thus was solved to obtain absorption.

\[ T = e^{-\alpha t} \quad \text{Eqn. 9} \]
Subsequently, inputting the wavelength and absorption obtained just above, the extinction coefficient can be found using this equation:

\[ k = \frac{\alpha \lambda}{4\pi} \]  

Eqn. 10

In Figure 67, both n and k values for tin dioxide can be observed with a cross point wavelength of 282 nm yielding an index of 0.35 [30].

![Image: Thickness measurement of SnO₂ on sapphire.](image)

Figure 66. Thickness measurement of SnO₂ on sapphire.
**Figure 67.** Refractive and extinction coefficients for tin dioxide.

### 8.3. Band Gap Calculation

Based on the work of Torres and Ordonez who studied the optical properties of cadmium sulfide, the band gap of tin dioxide was obtained using a linear least square fit [31],[32]. Using the relationship of photon energy with absorption that relates wavelength energy \((E)\), absorption\((\alpha)\), band gap energy \((E_G)\) plus a modifying constant \((C)\)

\[
(E\alpha)^2 = C^2E - C^2E_G
\]

Eqn. 11

an equation with the linear form of \(Y=mX+b\) can be fitted by looking at absorption and determining where it dominates. In Figure 68, it is clear that absorption becomes dominant from 4eV to 6eV. Subsequently, \((E\alpha)^2\) against wavelength energy is plotted (Figure 69) and linear least squares fit is performed for the range this energy range. By choosing one point of the line and using Eqn. 11, band gap energy is solved which gives a value of 3.99eV for tin dioxide.
Figure 68. Tin dioxide absorption versus wavelength energy.

Figure 69. \((E\alpha)^2\) and first degree least square fit for \((E\alpha)^2\)
9. Preliminary Results of Printed Ag TE Contacts

An approach taken to create a more industrial like system for the Ti/SnO2/Ag memristor was to print the Ag TE. Support for this process has been the specialty of another UTEP laboratory: the W.M. Keck Center. For this platform, RF sputtered SnO2 films over Ti were provided on Kapton and glass, and the Keck Center, using a Dimatix-2800 printer, deposited Ag contacts (Figure 70). An SEM image of a squared .8mm² contact can be observed in Figure 71, a contact that has a thickness of 1.54μm.

![Figure 70. Printed Ag TE memristor on glass.](image1)

![Figure 71. SEM image of a printed Ag TE contact for a memristor on Kapton.](image2)
Integration of a printed Ag TE contact was found to be more challenging than expected. Incompatibility of the surface energies and the nanoparticle and organo-metallic silver inks made difficult to print on the tin oxide surface. More importantly, the electrical behavior of these cells was not the same to the hand-applied contacts. Figure 72 was the best IV plot obtained. However, desirable traits were shown by these memristors, endurance shows higher LRS mean resistance of 725Ω, but at the same time HRS resistance is even higher for a corresponding mean resistance of 271K Ω. These values yield a larger HRS/LRS ratio of 371 compared to the memristors with hand-applied TE contacts.

Figure 72. IV behavior for memristor on Kapton with printed Ag TE.
Another important aspect that can be observed in the IV plots (Figure 72) is the higher set and reset voltages (Figure 74) that printed Ag contacts showed: set voltages with a mean of 5.2V and a mean reset voltage of 1.9V. An effect on HRS that was observed through the printed memory cells is a tendency of set voltage to increase. In Figure 75 the LRS plots were eliminated, so the predisposition of this memristor on the HRS can be observed more clearly.
Figure 74. Set and Reset Voltages for memristor on Kapton with printed Ag TE

Figure 75. Set voltage increase for memristor on Kapton with printed Ag TE
10. Conclusions & Future Work

This work provides a comparison between SnO$_2$ memristors fabricated on glass and Kapton substrates. Interestingly, no major drawback or difference between both substrates was observed in the resistive switching mechanism. However, lower yield of functional devices was observed with the Kapton devices and this is attributed to the scratches on the film that were reported on this document. Therefore, the SnO$_2$ memristor shows substrate independence and also it was proven that the mechanism can still work even if the substrate is not at its best conditions.

Another milestone for this work is the contribution of printed Ag TE contacts; this is a feature that may lead to inexpensive manufacturing of flexible memories. Although, the memristors with Ag TE did not behave as good as the hand applied contacts, the system has been demonstrated. Besides, fabrication of this system may be improved to optimize its behavior. First, the same Ag ink used for the hand applied contacts is recommended to be used as the chemicals found in the organo-metallic and nano particle based inks may be affecting the system. Another possibility is to tune the thickness of SnO$_2$ for these types of inks. Moreover, characterization needs to be improved for further understanding of the printed Ag TE memristors. It was observed that different compliance currents to the ones available may provide stability to the device, while larger voltages may be required for set voltages as it is inferred in Figure 75.

Optical characterization and structural analysis paves the road for a type of electrical characterization not observed in the journals read by the author. SnO$_2$ is a compound that can behave as metal or semiconductor by controlling its doping. Therefore, a study correlating doping of SnO$_2$ and its impact on its electrical behavior can be done by linking the band gap of tin dioxide and the electrical behavior.

One step further in this research line is to create a cross bar tin dioxide memory using lithography or shadow masks in the titanium layer and creating transversal Ag printed lines to form a cross-bar architecture (Figure 76). Moreover, if TE and BE can be printed and by incorporating a solution based spun coat MO like tin dioxide or titanium dioxide an inexpensive process could be conceived.
Another aspect that needs to be explored and is still not well understood is physical mechanism for resistive switching. SEM imaging at high magnifications might be able to detect eruptions or conduction paths on tin dioxide films. Moreover, if the mechanism relies on moving homogenous mechanism, surface elemental analysis with XPS or other comparable approaches might see a difference before and after exciting the device. Since only Ag can be easily removed and it is still possible that the mechanism manifests either at the titanium boundary or in between the MO layer, HRTEM cross section should also be performed to detect any physical change or ion movement.

Automating electrical characterization is advised as it can obtain real endurance and retention values, as the memristors did not fail in the current range. Another important aspect to explore is to expose the devices to radiation and characterize the effects that it has on the switching mechanism. Furthermore, Kapton memristors need to be characterized comparing retention, endurance and set and reset voltages while bending is introduced.
References


Curriculum Vita

Son of Oscar Del Real Ramirez and Socorro Uribe Carreon, Oscar Del Real Uribe was born in Hgo. Del Parral, Chih, MX. He lived for 18 years in Santa Barbara, Chih.Mx until decided to pursue the Degree of Electrical and Computer Engineering in 2004. At the beginning of 2007, Oscar began to work as an undergraduate research assistant in NanoMIL thanks to the advice of David Zubia. During the summer of 2007, thanks to the Austin Community College and the Texas Nanofuture program, Oscar attended an internship with ATDF as an interconnect manufacturing technician. Oscar graduated from his Bachelor degree in the spring of 2009, after which immediately, joined TI Dallas as a Development Engineer in a MEMS fab. In August 2009, Oscar began pursuing his Masters in Science in Electrical Engineering, a journey that would take him from solar cells research to high-k dielectrics and finally to memristors. In the summer 2010, Oscar joined TI Houston to work as an intern SOC Design Engineer for the summer. From fall 2010 to spring 2011, Oscar performed research on printed and flexible memristors that would eventually become his thesis topic.

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